ABSTRACT OF THE DISCLOSURE

A semiconductor integrated circuit, including a test scan arrangement has a plurality of scan chains arranged in pairs. These scan chains have input terminals for receiving test patterns, and outputs provided to compression logic such as a distributed XOR tree multiple input shift register to provide an output which is a compressed signal derived from the output test patterns. In an alternative configuration, the first scan chain of each pair is connected to the second scan chain of each pair, and the input terminal of the second scan chain becomes the output terminal. Thereby creating a longer scan chain of the first and second scan chains together with one input terminal and one output terminal. The two loads allow for efficient scanning in the first mode, or debugging to determine the position of a fault in the second mode.